CLAIM AMENDMENTS

1 - 3. (Cancelled).

4. (Currently Amended) ~~The current controlled sense current source of claim 2 further comprising, in combination:~~ A current controlled sense current source for a magnetoresistive random access memory comprising:

a current source having a stable reference current output;

a sense current source having a sense current reference input connected to the stable reference current output with the sense current source having a sense current output;

bias tuning circuit comprising, in combination:

a bias generator having a bias output;

a plurality of switches having a word reference input and a mirror transistor output;

a plurality of mirror transistors connected to one of the mirror transistor outputs;

a transistor connected in a mirror configuration with the plurality of mirror transistors having a tuned reference output;

a selector to select one of the mirror transistor to activate the transistor to set the voltage to the plurality of mirror transistors;

a pad; and

a indicator transistor in a mirror configuration with the transistor connected to the pad to provide an indicator.

5. (Original) The current controlled sense current source of claim 4 with the pad being an external pad.

6. (Original) The current controlled sense current source of claim 4 with the indicator transistor having a gain that is a multiple of the transistor.

7. (Currently Amended) The current controlled sense current source of claim [[2]] 4 with the plurality of mirror transistors are n-channel transistors.

8. (Currently Amended) The current controlled sense current source of claim [[2]] 4 with the plurality of switches being transistors.

9. (Currently Amended) The current controlled sense current source of claim [[2]] 4 with the transistor being an N-channel transistor.

10. ~~The current controlled sense current source of claim 2~~ A current controlled sense current source for a magnetoresistive random access memory comprising:

a current source having a stable reference current output;

a sense current source having a sense current reference input connected to the stable reference current output with the sense current source having a sense current output;

bias tuning circuit comprising, in combination:

a bias generator having a bias output;

a plurality of switches having a word reference input and a mirror transistor output;

a plurality of mirror transistors connected to one of the mirror transistor outputs;

a transistor connected in a mirror configuration with the plurality of mirror transistors having a tuned reference output;

a selector to select one of the mirror transistor to activate the transistor to set the voltage to the plurality of mirror transistors;

with the bias generator being a temperature and voltage compensated bias generator.

11. (Currently Amended) The bias turning circuit of claim [[2]] 4 with the selector selecting one of the plurality of mirror transistors to ~~compenstate of~~ compensate for a tested parameter.

12. (Currently Amended) The current controlled sense current source of claim [[2]] 11 with the tested parameter being a manufacturing variance.

13 - 23. (Cancelled)